CALYPTO® | PowerPro Product Family Datasheet

KEY BENEFITS

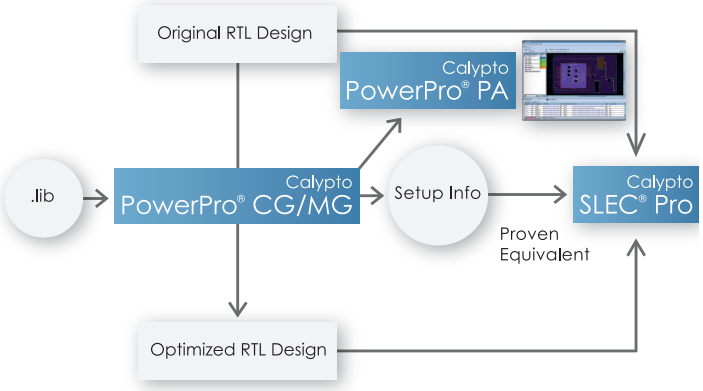
- RTL power optimization across entire SoC with automatic clock gating, memory gating and light sleep controller generation
- Up to 60% power savings from our patented sequential analysis technology
- Upfront RTL power estimation using built in logic synthesis engine
- Eliminate design risk with automatic formal verification using Calypto's SLEC Pro product
- User control and flexibility through automatic and guided power optimization flows
- Supports late design changes through PowerPro ECO flow
- Certified integrations with leading RTL Synthesis tools
- RTL power exploration through graphical analysis with TCL command line interface

INTRODUCTION

With the explosion of consumer electronics, designing for low-power has become an important design constraint and a key differentiating factor. The RTL design phase provides the ideal opportunity to dramatically reduce power, since several micro-architectural transformations can be done at this stage, both via automated tools as well as manually by the RTL designers. Also, power analysis can be done with reasonable accuracy at the RTL level to drive low power optimizations. Unlike combinational power optimization tools that only work at the gate level, PowerPro operates on the RTL thus giving the user the best opportunity to achieve the lowest power result.

SILICON-PROVEN PLATFORM FOR LOW-POWER SOC DESIGN

The PowerPro SOC Low-Power Platform is the leading RTL-level, power optimization toolset in the industry. Based on our patented sequential analysis technology, PowerPro looks at a design just like an engineer does, across clock and functional boundaries. Unlike other tools, PowerPro is not based on structural patterns in the design. PowerPro performs a functional analysis across multiple pipeline stages and analyzes the state machines in the design, enabling it to find the most advanced logic conditions possible to shut off redundant sections of a chip. PowerPro can be used to reduce power on the logic, memory, and core processor sections on an SOC.



KEY DIFFERENTIATORS

Unique Sequential Analysis Technology

Calypto's patented Sequential Analysis Technology allows PowerPro to consistently produce better results by order of magnitude in less time than manual RTL optimizations for power.

Next Generation Logic Synthesis Estimation Engine

PowerPro includes the next generation RTL logic synthesis estimation engine that estimates total power (static and dynamic) accurately thereby allowing the optimal power-performance tradeoff.

Automated RTL Generation

PowerPro automates the identification and insertion of sequential gating logic into the user's original RTL to dramatically reduce dynamic and leakage power.

Comprehensive Formal Verification

PowerPro optimized RTL is comprehensively verified with SLEC® Pro to guarantee that no functional changes are introduced. Additionally, because PowerPro MG maintains cycle-accurate behavior at the block boundary, existing simulation regressions can be used to verify PowerPro MG generated RTL.

Production Proven Flow Features

PowerPro has been used to minimize power of many taped SOC's in the market and has all the features required for supporting downstream implementation and verification.

-ECO
-Automatic CDC synchronizer identification
-Clock-domain aware reset logic insertion
-Customizability of PowerPro RTL to meet customers' lint rules guidelines
-Flow controls for scope of optimization in the design

PowerPro PRODUCT FAMILY

Calypto PowerPro® CG

Automatic + Manually Assisted Clock Gating

- Eliminating unnecessary toggles on clock network and flop outputs
- Power savings produced by PowerPro CG are complementary and cumulative to downstream power reduction tools used in synthesis, clock tree optimization, and physical design
- Power Adviser: Provides reports and hints to enable more potential to reduce power of the SOC through manual use mode

Calypto PowerPro® MG

Memory Power Reduction Through Memory + Light Sleep Gating

- Reduces dynamic power of the memory by shutting off memory during unnecessary memory accesses
- Reduces leakage power by inserting logic to control power-modes of memory
- Sequential analysis in PowerPro MG ensures that the memory is taken out of sleep modes adequately before memory access
- PowerPro MG prototyping technology performs the optimal tradeoff to maximize leakage power savings while minimizing toggling of sleep modes
- Allows flexibility of inserting the memory-gating logic to be inserted in user-specified datapath blocks, thereby preserving the memory hierarchy

Calypto PowerPro® PA

RTL Power Analysis + Sequential Optimization Visualization

- PowerPro Power Analyzer (PA) provides detailed hierarchical power reports of dynamic and leakage power consumed by logic, registers, memory and clock-tree
- Fast register-transfer level (RTL) power analysis
- Accurate within 15% of gate level
- Sequential analysis based switching activity propagation engines deliver precise switching activity information for all signals
- Under the hood logic synthesis engine to ensure the design database used for power analysis provides an accurate representation of the final synthesized design
- Advanced clock-gating aware clock-tree synthesis provides accurate clock-tree power
- Power information is reported in the context of RTL source code, schematic display, design hierarchy, and various sortable reports (ASCII, HTML, CSV, XML) to enable efficient design for low-power
- Allows visualization of sequential optimizations for manual and automated PowerPro flows by way of schematics, reports and embedded expressions in the original RTL

SYSTEM REQUIREMENTS AND COMPATIBILITY

Languages:

VHDL 87, 93 & 97 and Verilog 95 & 2001, SystemVerilog, SystemC 2.1 and 2.2

Platforms:

Redhat Enterprise Linux 4.0, 32-bit and 64-bit x86 compatible hardware, 2 GB minimum

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