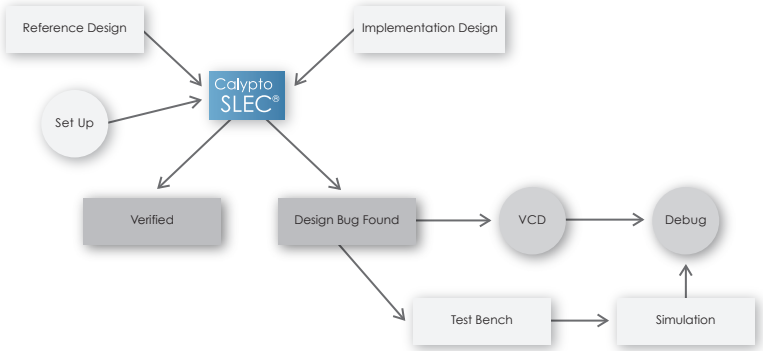
CALYPTO® | SLEC Product Family Datasheet

KEY BENEFITS

- Formally verifies two sequentially different designs are functionally equivalent
- Verifies without testbenches or assertions
- Integrates with industry leading high-level synthesis tools
- Leverages system-level models to verify RTL designs
- Quickly finds bugs that other tools miss
- Isolates bugs with short, concise debug waveforms
- Ensures Hardware intent remains unchanged during system-level model refinement
- Replaces time consuming simulation regressions with fast results
- Enables aggressive RTL power and timing optimizations by providing formal verification sign-off
- Does not require 1-1 state point or I/O maps



INTRODUCTION

The emergence of consumer electronics is causing a fundamental shift in Register Transfer Level (RTL) design methodologies. The race for time to market has resulted in the adoption and growth of higher level design creation methodologies. In particular, High Level Synthesis (HLS) directly from software models to hardware has become very popular. On the other end of the spectrum, the need to create faster and lower power RTL designs for consumer devices has led to design flows where designers use aggressive techniques for optimizing a given RTL design. However these new design techniques create new challenges for verification. There is a significant need for next generation equivalence checking solutions which verify software models against the HLS generated RTL, as well as various optimized versions of an RTL design against the original RTL. Traditional combinational equivalence techniques are not applicable to these next generation problems.

FUNCTIONAL VERIFICATION ON A NEW LEVEL

SLEC is the only sequential logic equivalence checking family available in the industry today. Based on our patented Sequential Analysis Technology, SLEC designs with different abstraction levels, internal states, timing, and interfaces. By verifying that both designs produce the same output for all possible inputs, over all time, the quality of verification that SLEC performs in minutes is equal to years of running simulation. Because SLEC does not require testbenches or assertions, engineers spend significantly less time developing their verification environment and more time creating quality designs. The SLEC family consists of three products:

- SLEC Pro provides automatic sequential formal equivalence checking between the original RTL going into PowerPro, and the lower-power RTL produced by PowerPro.
- SLEC RTL functionally verifies two RTL designs with sequential differences. Common examples of this are when clock gating is manually added to reduce power, or when the pipeline structure is changed to increase performance. This is a very normal practice when designing an SOC based on ARM processors.
- SLEC HLS is used to automatically compare C to C, and C to RTL, in today's High-Level Synthesis flows. It is integrated with the leading HLS tools in the market (Calypto's Catapult, Cadence C-to-S, Forte Cynthesizer).

KEY DIFFERENTIATORS

Strong Sequential Proofs Engine

Strong sequential proofs engine which deploys techniques like induction for complete proof for designs with complex states.

Unique Word Level Solvers

Unique word level solvers which are critical for equivalence checking of designs with complex control and arithmetic.

Hardware Model Extraction

Hardware model extraction from software languages like C/C++.

Integration with HLS Products

Tight integration with HLS products (Catapult, Cadence CtoS, Forte Cynthesizer) for a completely automated synthesis and equivalence checking flow.

Prodution Proven Flow Features

Production proven with over 100 tapeouts across all industry segments and design types.

Sampling of Blocks Verified by SLEC

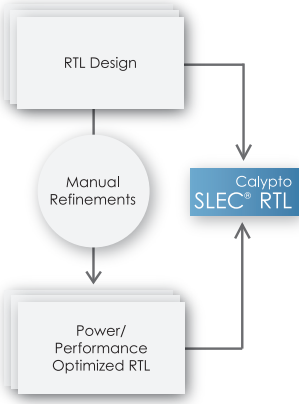
Instruction pipeline: ARM. MIPS, PowerPC, SH, V850, DSP: C-XX, MPEG4 dct/idct, H.264 interleaver, wireless baseband DSP, weiner filter, encryption, video mapper, ultra wideband filter, floating point unit, 3D graphic processor, arithmetic logic unit, memory cache, gaussian filter, audi encoder/decoder, vector processor, audio equalizer, amd PCI express core.

SLEC PRODUCT FAMILY

Calypto SLEC® RTL

Popular Application: Verification of RTL Level Power and Timing Optimizations for ARM Cores

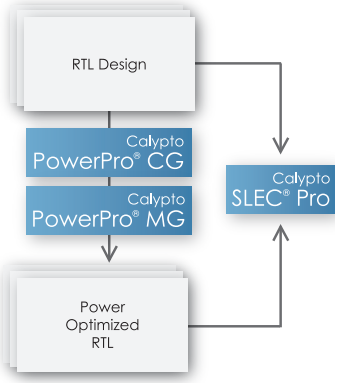
SLEC RTL is a good fit for high performance and low power RTL design teams. With SLEC RTL designers can make aggressive optimizations which often involve micro-architectural changes to the RTL blocks. In particular merging or splitting flops, re-encoding states, re-pipelining, retiming and clock gating can be completely and exhaustively verified by SLEC RTL without the need for time consuming simulations. The figure bellow shows some of the transforms verified by SLEC RTL. Design teams working on microprocessor cores use it for verifying all functionality preserving manual RTL edits before checking them in. This lends stability to the full chip regressions and takes significant workload away from simulation farms. SLEC RTL has been used in multiple processor tapeouts and is a very popular solution for ARM core RTL optimization teams.



Calypto SLEC® Pro

Popular Application: Verification of Power Optimized RTL Generated by PowerPro®

SLEC Pro is a fully automatic formal verification solution for RTL blocks optimized by Calypto's PowerPro SoC low power design platform. It comes with unique technology specifically targeted for the class of power optimizations performed by PowerPro CG and PowerPro MG. It is currently used as a standard verification solution by almost all PowerPro customers.



SYSTEM REQUIREMENTS AND COMPATIBILITY

Languages:
VHDL 87, 93 & 97 and Verilog 95 & 2001, SystemVerilog, SystemC 2.1 and 2.2

Platforms:
Redhat Enterprise Linux 4.0, 32-bit and 64-bit x86 compatible hardware, 2 GB minimum

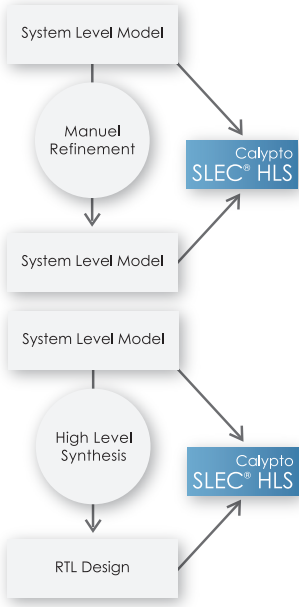
HLS Integrations: Calypto's Catapult, Cadence C-to-S, Forte Cynthesizer

Simulation and Debug Environment: Novas Debussy/Verdi, Cadence NC/Simvision, Synopsys VCS, Mentor's Modelsim/Questa

Calypto SLEC® HLS

Popular Applications: HLS Sign-off Checking for Catapult, Cadence C-to-S and Forte Cynthesizer

SLEC HLS is a good fit for all design teams which are using High Level Synthesis as part of their RTL design flow. It is fully integrated with the above mentioned industry standard HLS tools resulting in an easy to use synthesis and verification flow. It provides a comprehensive signoff of the RTL functionality generated by HLS and is a key enabler in the adoption of HLS. C-C equivalence checking is another very useful application of SLEC HLS. The need for this verification arises often in a HLS flow where the C/SC model is refined multiple times to get the best quality of results from HLS. SLEC HLS is used to ensure that no refinement iteration compromises the original functionality. The figure bellow shows the two use models of SLEC HLS in the design flow.



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