KEY BENEFITS

- SystemC and ANSI C++ synthesis
- Mixed datapath and control logic synthesis
- Multi-abstraction synthesis
- Power, performance, and area optimization
- Push-button generation of RTL verification infrastructure
- Top-down and bottom-up hierarchical design management
- Full and accurate control over design interfaces
- AXI interface library
- Silicon vendor certified synthesis libraries
- Integrated ECO and formal verification

ACCELERATE TIME TO RTL, REDUCE VERIFICATION EFFORT

Traditional hardware design methods that require manual RTL development and debugging are too time consuming and error prone for today's complex designs. The Catapult® high-level synthesis tool empowers designers to use industry standard ANSI C++ and SystemC to describe functional intent, and move up to a more productive abstraction level. From these high-level descriptions Catapult generates production quality RTL. With this approach, full hierarchical systems comprised of both control blocks and algorithmic units are implemented automatically, eliminating the typical coding errors and bugs introduced by manual flows. By speeding time to RTL and automating the generation of bug free RTL, the Catapult significantly reduces the time to verified RTL.

Catapult's unified flow for modeling, synthesizing, and verifying complex ASICs and FPGAs allows hardware designers to fully explore micro-architecture and interface options. Advanced power optimizations automatically provide significant reductions in dynamic power consumption. The highly interactive Catapult workflow provides full visibility and control of the synthesis process, enabling designers to rapidly converge upon the best implementation for performance, area, and power.

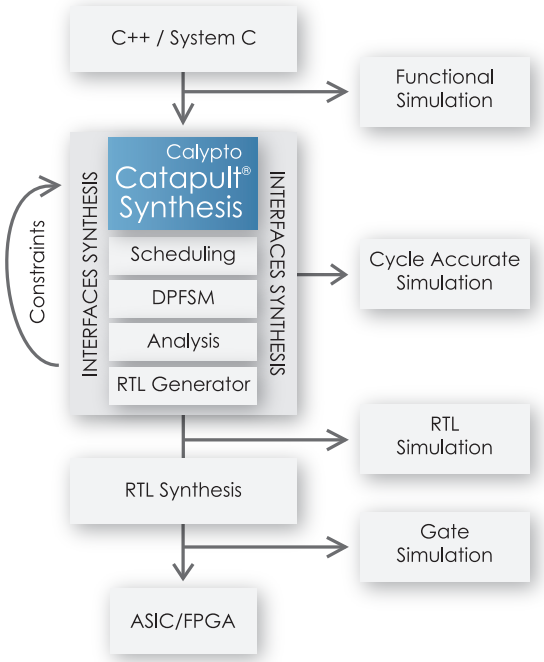
KEY DIFFERENTIATORS

High-Level Synthesis from ANSI C++ and SystemC

Catapult offers support both for pure untimed ANSI C++ and for SystemC, so companies can leverage legacy designs.

Hierarchy Synthesis

Catapult synthesizes multi-block pipelined and concurrent hierarchical designs from pure sequential ANSI C++ and SystemC.



Front-to-Back, Fully Automated Verification

Catapult integrates a push-button, fully automated verification flow that produces all the required files and scripts to verify a generated design. Both functional simulation and formal methods for verification are integrated with Catapult.

Micro-Architecture Analysis and Optimization

Catapult combines automation with specific high-level constraints so designers can precisely control the hardware implementation and interactively converge on the best hardware architecture.

Interface Synthesis

Catapult accepts pure ANSI C++ description as its input and uses patented interface synthesis technology to control the timing and communications protocol on the design interface, so designers can can explore a full range of hardware interface options without changing the source.

SystemC Modular IO

Catapult synthesizes abstract SystemC transaction models as well as lower abstraction cycle accurate models. Leveraging Catapult Modular IO library, customers can easily specify point-to-point block interconnect without degrading simulation speed or hardware quality. The standard interconnect includes point-to-point handshake, FIFO and memories. Catapult also supports custom IO written in standard SystemC and can even support complex bus interfaces. Modular IO libraries simplify writing, debugging and integrating designs by giving a consistent way to define and use interfaces.

AXI Interface Library

Leverage Catapult's Modular IO standard, Calypto also offers the industry's first production quality AXI bus bridge for easily connecting hardware subsystems to ARM platforms. The libraries include master and slave interfaces with both Transaction Level Modeling (TLM) and HLS views, which allows easy interplay between a TLM 2.0 platform and HLS implementation flow without degrading simulation performance or hardware quality. The highly parameterizable AXI interface supports a wide range of configurations including burst modes, bus width and auxiliary control signals.

Low-Power Exploration and Optimization

Catapult LP (low power) takes advantage of Calypto's leading PowerPro technology under the hood to seamlessly produce the lowest power RTL and deliver up to 80% power savings at the architectural level. Starting with SystemC or C++, Catapult LP performs power estimation, architectural power optimizations and fine grain sequential clock gating. With Catapult LP designers can explore different hardware architectures, including various memory banking schemes, to produce the ultimate in low power hardware designs.

Integrated ECO and Formal Verification

Calypto's offers an integrated ESL design flow which tightly couples Catapult for high level synthesis with SLEC for sequential formal equivalence checking. The flow dramatically reduces time to design and verify hardware subsystems. Calypto's ESL design flow connects SystemC TLM 2.0 virtual platforms, system verification and emulation by partnering with Mentor and other EDA providers. After more than 1000+ ASIC tapeouts, Calypto has solidified its production quality integration with DesignCompiler for predictable timing closure and Conformal ECO for engineering change orders.

Predictable Timing Closure

Catapult features technology-aware scheduling and allocation heuristics to produce superior designs and predictable timing closure in the physical design stage.

CATAPULT PRODUCT FAMILY

Calypto Catapult® SL

System Level Hierarchy Synthesis

- Top down and bottom up hierarchy synthesis for multimillion gate subsystem design
- Dramatically shortens the design cycle by producing correct-by-construction designs, error-free RTL generation, and zero iterations at the RTL
- Synthesizes ANSI C++ and SystemC to production quality RTL
- Targets algorithms, control logic, and interfaces for subsystem design
- Delivers optimal implementations within aggressive time-to-market requirements
- Enables precise control of the synthesized hardware implementation by applying high-level constraints to manage interface protocols, memory architecture, through put, latency, and low-power transformations
- Yields immediate and measurable benefits with the fastest path to verified RTL, more gates produced per engineer, and positive ROI on the first design

Calypto Catapult® LP

C to RTL Low Power HLS

- All features of Catapult SL plus low power optimization
- Built in C++/SystemC power estimation achieves up to 80% power reduction at the architecture level
- Sequential clock gating for fine grain power reduction of register, clock tree, and logic power
- Memory architecture optimization reduces memory power up to 80% with memory banking exploration and optimization
- Leverages Calypto's leading PowerPro technology under the hood to seamlessly produce the low power RTL
- Provides SystemC/C++ power estimation

SYSTEM REQUIREMENTS AND COMPATIBILITY

Languages: VHDL 87, 93 & 97 and Verilog 95 & 2001, system verilog
Platforms: Windows NT/2000/XP, Linux Red Hat Enterprise, and SUN Solaris 8
Operating Systems: Redhat Enterprise Linux 3.0 and 4.0
Memory: 2 GB minimum

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